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| 10/803,475 | 03/18/2004 | James A. Cunningham | 61011 | 5511 |

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ALLEN, DYER, DOPPELT, MILBRATH & GILCHRIST P.A.
1401 CITRUS CENTER 255 SOUTH ORANGE AVENUE
P.O. BOX 3791
ORLANDO, FL 32802-3791

| EXAMINER | |
|---|---|
| SMOOT, STEPHEN W | |
| ART UNIT | PAPER NUMBER |
| 2813 | |

DATE MAILED: 06/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/803,475 | CUNNINGHAM, JAMES A. | |
| | Examiner | Art Unit | |
| | Stephen W. Smoot | 2813 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *18 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,2 and 7* is/are allowed.

6)☒ Claim(s) *3,4,6,8-10 and 13-16* is/are rejected.

7)☒ Claim(s) *5,11,12 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

This Office action is in response to application papers filed on 18 March 2004.

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 6 recites the limitation "said second diffusion barrier layer" in lines 17-18.

There is insufficient antecedent basis for this limitation in claim 6.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 6, 8-9, 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Avanzino et al. (US 6,469,385 B1).

Referring to Fig. 3 and column 5, line 11 to column 6, line 44, Avanzino et al. disclose an interconnect structure that includes the following features:

- A semiconductor wafer (200) that includes first and second channels (202, 204) (i.e. trenches) connected by a via (206);
- The first channel (202) is embedded in a first dielectric layer (208) and includes a first conductor core (230) that can be copper lined with a first seed layer (228) that can be a copper alloy;
- A via stop layer (220) (i.e. a cap) on the conductor core (230);
- A second dielectric layer (212) over the via stop layer (220);
- A channel stop layer (222) over the second dielectric layer (212);
- The via (206) is over the conductor core (230) and through the via stop layer (220);
- The sides of the via (206) and the second channel (204) are surrounded by a region of SiC(H) barrier material (231);
- The via (206) and the second channel (204) are lined with a second seed layer (234) that can be a copper alloy and are filled with a second conductor core (236) that can be copper;

- Oxygen gettering layers (226, 232) are optional, so the second seed layer (234) can be in direct contact with the first copper core (230); and
- The SiC(H) barriers are formed by reducing exposed surfaces of dielectric layers (216, 208, 212, 210), which implies that the channel stop layer (222) is a different material that is also capable of functioning as a diffusion barrier layer since some portions would be in direct contact with the second seed layer (234) when the gettering layers (226, 232) are not used.

These are all of the limitations set forth in claims 6, 8-9, 13 of the applicant's invention.

5. Claim 8 is rejected under 35 U.S.C. 102(b) as being anticipated by Nguyen et al. (US 5,904,565).

Referring to Fig. 18 and column 8, line 59 to column 10, line 53, Nguyen et al. disclose an interconnect structure for an integrated circuit (160) that includes the following features;

- A first metal level (162) (i.e. a substrate);
- A first dielectric layer (166) over the first metal level (162);
- A first trench (172 in Fig. 17) in the first dielectric layer (166) that is lined with a third barrier layer (186) that can be a conductive material like refractory materials or refractory metal compounds and is typically filled with copper (188);
- A second dielectric layer (192) with a dual damascene opening corresponding to a second via (200) and a second trench (206) over the copper-filled trench (188);

- A sixth barrier layer (214) over sidewalls of the second via (200) and the second trench (206); and
- A fifth barrier layer (212) covering horizontal surfaces of the second trench (206);
- The fifth barrier layer (212) is non-conductive, while the sixth barrier layer (214) can be conductive (also see column 12, lines 6-17), in which case they would be different materials.

These are all of the limitations set forth in claim 8 of the applicant's invention.

6. Claims 15-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Barr et al. (US 2002/0093098 A1).

Referring to Fig. 12 and paragraphs [0022] to [0026], Barr et al. disclose an interconnect structure that includes the following features:

- A semiconductor substrate (100) (also see paragraph [0009]);
- A dielectric layer (124) over the substrate (100) that is embedded with a dual damascene via/trench structure comprising a copper fill (128) with an adhesion/barrier liner (126) of a refractory metal and/or refractory metal nitride (also see paragraphs [0010] to [0011]);
- A conductive barrier layer (82) formed over the copper fill (128) that can be a conductive metal oxide with corresponding metal like ruthenium with ruthenium oxide (also see paragraph [0013]); and

- A passivation layer (92) that is typically silicon nitride, silicon oxynitride, or silicon dioxide (i.e. a dielectric layer) is formed over the conductive barrier layer (82) and the dielectric layer (124).

These are all of the limitations set forth in claims 15-16 of the applicant's invention.

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nguyen et al. (US 5,904,565) in view of Ting et al. (US 5,969,422).

Referring to Fig. 18 and column 8, line 59 to column 10, line 53, Nguyen et al. disclose an interconnect structure for an integrated circuit (160) that includes the following features;

- A first metal level (162) (i.e. a substrate);
- A first dielectric layer (166) over the first metal level (162);

- A first trench (172 in Fig. 17) in the first dielectric layer (166) that is lined with a third barrier layer (186) that can be a conductive material like refractory materials or refractory metal compounds and is typically filled with copper (188);
- The copper-filled trench (188) is covered with a fourth barrier layer (190);
- A second dielectric layer (192) with a dual damascene opening corresponding to a second via (200) and a second trench (206) over the fourth barrier layer (190);
- The second via (200) extends through the fourth barrier layer (190) to the copper-filled trench (188);
- A fifth barrier layer (212) covering horizontal surfaces of the second dielectric layer (192) including the bottom of the second trench (206) that is formed of a non-conductive material like silicon nitride (also see column 12, lines 6-13);
- A sixth barrier layer (214) over sidewalls of the second via (200) and the second trench (206) that can be formed of a conductive material (also see column 12, lines 6-17); and
- The second via (200) and the second trench (206) are typically filled with copper (also see column 11, line 58 to column 12, line 17).

These are limitations set forth in claim 3 of the applicant's invention.

However, Nguyen et al. do not expressly teach or suggest an alloy seed layer that comprises copper over the conductive diffusion barrier, which is also a limitation of claim 3. More specifically, Nguyen et al. do not expressly teach or suggest an alloy seed layer that comprises copper and at least one of tantalum, molybdenum, chromium,

and tungsten, which is the further limitation to claim 3 as set forth in claim 4 of the applicant's invention.

Ting et al. teach a copper seed layer (14, 22) that is alloyed with a refractory metal like tantalum, molybdenum, chromium, or tungsten (advantageously copper alloyed with either tantalum or tungsten) that can be used for plating copper interconnects (15, 23) (see Fig. 2, column 6, lines 56-65, and column 8, line 65 to column 9, line 30).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Nguyen et al. and Ting et al. in order to use a copper tantalum or copper tungsten seed layer, as taught by Ting et al., for filling the dual damascene openings of Nguyen et al. with copper by plating. Ting et al. recognize numerous advantages for using a copper tantalum or copper tungsten seed layer including improved step coverage, the capability of functioning as a barrier layer, and improved adhesion (see column 11, line 59 to column 12, line 7).

9. Claims 10, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Avanzino et al. (US 6,469,385 B1) as applied to claims 9, 13 above, respectively, and further in view of Ting et al. (US 5,969,422).

As shown above, Avanzino et al. anticipate claims 9, 13 of the applicant's invention. However, Avanzino et al. do not expressly teach or suggest an alloy seed layer that comprises copper and at least one of tantalum and chromium, which are the further limitations to claims 9, 13 as set forth in claims 10, 14, respectively, of the

applicant's invention. Ting et al. teach a copper seed layer (14, 22) that is alloyed with a refractory metal like tantalum or chromium (advantageously copper alloyed with tantalum) that can be used for plating copper interconnects (15, 23) (see Fig. 2, column 6, lines 56-65, and column 8, line 65 to column 9, line 30).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Avanzino et al. and Ting et al. in order to use a copper tantalum seed layer for plating copper, as taught by Ting et al., to form the copper cores of Avanzino et al. Ting et al. recognize numerous advantages for using a copper tantalum seed layer including improved step coverage, the capability of functioning as a barrier layer, and improved adhesion (see column 11, line 59 to column 12, line 7).

***Allowable Subject Matter***

10. Claims 1-2, 7 are allowed.

11. Claims 5, 11-12, 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter:

- Claims 1-2 are allowed because the prior art of record does not teach or suggest, in combination with the other claim limitations, an integrated circuit that includes a cap layer comprising metal on a first conductive region comprising copper within a trench, combined with a via over the first conductive region and through the cap layer, wherein an alloy seed layer comprising copper and at least one of tantalum, molybdenum, chromium, and tungsten is over a diffusion barrier layer on sidewalls of the via and wherein the alloy seed layer is in contact with the first conductive region;
- Claim 5 would be allowable because the prior art of record does not teach or suggest, in combination with the other claim limitations, an integrated circuit that includes a cap layer comprising metal on a first conductive region comprising copper within a trench, combined with a via over the first conductive region and through the cap layer, wherein an alloy seed layer comprising copper is over a conductive diffusion barrier layer on sidewalls of the via and wherein the alloy seed layer is in contact with the first conductive region;
- Claim 7 is allowed because the prior art of record does not teach or suggest, in combination with the other claim limitations, an integrated circuit that includes a cap layer comprising at least one of palladium and platinum on a first conductive region comprising copper within a trench, combined with a via over the first conductive region and through the cap layer, wherein an alloy seed layer comprising copper and at least one of tantalum, molybdenum, chromium, and

tungsten is over a third diffusion barrier on sidewalls of a via and the alloy seed layer is in contact with the first conductive region;

- Claims 11-12 would be allowable because the prior art of record does not teach or suggest, in combination with the other claim limitations, an integrated circuit that includes a cap layer comprising at least one of palladium and platinum on a first conductive region comprising copper within a first trench, combined with a first diffusion barrier over via and second trench sidewalls corresponding to a dual damascene opening and combined with a second diffusion barrier over horizontal surfaces of the second trench opening, wherein the first diffusion barrier and the second diffusion barrier are different materials; and
- Claim 17 would be allowable because the prior art of record does not teach or suggest, in combination with the other claim limitations, an integrated circuit that includes a diffusion barrier/cap layer comprising a metal and a conductive oxide of the metal over a first conductive region comprising copper within a trench, combined with a layer of silver and a layer of palladium between the diffusion barrier/cap layer and the first conductive region.

## *Conclusion*

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Maniar et al. teach a rhenium with rhenium oxide cap layer. Ngo et al. teach copper alloy seed layers. Nakano et al. teach an interconnect structure that

features forming a via through a metal cap. Chung teaches an interconnect structure that features a conductive barrier formed on sidewalls.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 571-272-1698. The examiner can normally be reached on M-F (8:00 am to 4:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sws

Stephen W. Smoot
Patent Examiner
Art Unit 2813